REMARKS

This is in response to the Office Action dated July 27, 2005.

The title has been amended. See section 2 of the Office Action. It is respectfully submitted that the title is descriptive of example embodiments.

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Taki in view of Yonemaru. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires that "a predetermined scheme is used to connect between the first cell and the second cell, between the plurality of transistors in the first cell, and between the PMOS transistor section and the NMOS transistor section in the second cell, and wherein the first cell functions as a logic operation circuit for outputting data, and the second cell functions as at least one of a driver circuit for driving the logic operation circuit or a data retaining circuit for retaining data output by the logic operation circuit." The cited art fails to disclose or suggest these features of claim 1.

The Office Action *admits* that Taki fails to disclose or suggest that the second cell functions as at least one of a driver circuit for driving the logic operation circuit (claim 1) or as a data retaining circuit for retaining data output by the logic operation circuit (claim 24). Taki discloses a logic gate cell featuring a small area and low power consumption which is constructed of a circuit of two inverting logic gates connected in series in a layout of four-step diffusion regions (e.g., see Abstract of Taki). In particular, the inverting logic gates refer to a NAND gate, a NOR gate, a NOT gate, and an AND-NOR compound gate and an OR-NAND compound gate (col. 1, lines 16-18). Taki discloses the circuit arrangement for the connection of the two inverting logic gates by employing two PMOS transistor diffusion regions and two

NMOS transistor diffusion regions, where the first inverting logic gate is realized by the two internal diffusion regions and the second inverting logic gate is realized by the two external diffusion regions (e.g., col. 2, lines 21-43). An output of the first inverting logic gate is connected to one of inputs of the second inverting logic gate. A particular scheme is used to connect between the first inverting logic gate and second inverting logic gate. In Figs. 49A and 49B, Taki discloses an AND-OR circuit with the circuit diagram shown in Fig. 50. The circuit diagram comprises a first inverting logic gate 1, which is connected to a second inverting logic gate 2. As shown in the circuit diagram, the first inverting logic gate 1 comprises a PMOS transistor section and an NMOS transistor section. Furthermore, the PMOS transistor second includes a first PMOS transistor and a second PMOS transistor connected in series. Similarly, the NMOS transistor section includes a first NMOS transistor and a second NMOS transistor connected in series. The connection scheme is shown in Figs. 47A, 47B, 48A and 48B.

As mentioned above, the Office Action *admits* that Taki fails to disclose or suggest that the second cell functions as at least one of a driver circuit for driving the logic operation circuit (claim 1) or as a data retaining circuit for retaining data output by the logic operation circuit (claim 24). The Office Action cites Yonemaru in an attempt to cure these deficiencies in Taki (see page 5 of the Office Action). The Office Action argues that it would have been obvious to have replaced Taki's second cell with another cell that functions as a data retaining circuit for retaining data output by the logic operation circuit (with citation to Yonemaru).

The Section 103(a) rejection is flawed. There is no suggestion or motivation in the art of record which would have caused one of ordinary skill in the art to have replaced Taki's second cell with another cell that functions as a data retaining circuit for retaining data output by the

logic operation circuit. Taki teaches away from this, and there is no reason why one would have modified Taki to meet the invention of claim 1 (or claim 24).

Yonemaru discloses a D flip-flop circuit FF1 that serves as a data storing circuit (see [0081]). The integrated circuit of Yonemaru includes MOSFETs of at least one of N channel and P channel types where at least two MOSFETs included in a plurality of MOSFETs include two serially-connected MOSFETs of the same channel-type in which their respective gates are connected to each other (e.g., see Abstract). Therefore, a leakage current flowing through the semiconductor integrated circuit can be decreased when not in operation according to Yonemaru (see [0019]).

Specifically, Yonemaru discloses methods of incorporating the NMOSFET m2 and/or PMOSFET m1 as shown in Figs. 1B and 1C respectively into an inverter logic circuit I1 as shown in Fig. 1A so that the leakage current in the circuit I1 can be reduced (see [0065] – [0069]). Furthermore, Yonemaru discloses methods of incorporating the inverter logic circuit I1 (which includes the NMOSFET m2 and/or PMOSFET m1) into circuits such as a pass transistor logic circuit or a D flip flop circuit so that the leakage current in the D flip-flop circuit FF1 can be decreased (see [0081] – [0087]).

Accordingly, there is a lack of motivation or suggestion in the art to combine the teachings of Taki with that of Yonemaru, as Taki teaches away from Yonemaru. Taki teaches a method that provides a high area-utilization and small-area logic gate cell which employs a layout that narrows a cell width to realize a low power consuming logic gate cell based on a narrow gate width transistor (col. 2, lines 20-25). In contrast, Yonemaru teaches different configurations of NMOSFET and PMOSFET (see Figs. 1B, 1C, 6B, 6C, 7B, 7C) that can be

incorporated into circuits such as an inverter logic circuit, a pass transistor logic circuit or a D flip flop circuit so that leakage current can be decreased.

Furthermore, Taki specifically states that it covers a logic gate cell that includes two inverting logic gates 1 and 2, with an output of the first inverting logic gate 1 connected to one of inputs of the second inverting logic gate 2. *The inverting logic gates refer to a NAND gate, a NOR gate, a NOT gate, an AND-OR compound gate and an OR-NAND compound gate as shown in Figs. 1-7 (see col. 9, lines 28-38). Thus, there is a lack of motivation to combine Taki with Yonemaru as the D flip-flop of Yonemaru is not an inverting logic gate as disclosed by Taki.* Accordingly, it is respectfully requested that the Section 103(a) combination rejection be withdrawn (as to all claims).

It is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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